UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,105	11/14/2003	Anthony Correale JR.	RPS920030130US1	1935

25299 7590 11/16/2006

IBM CORPORATION
PO BOX 12195
DEPT YXSA, BLDG 002
RESEARCH TRIANGLE PARK, NC 27709

EXAMINER	
PATEL, KAUSHIKKUMAR M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 11/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/714,105	CORREALE ET AL.	
	Examiner	Art Unit	
	Kaushikkumar Patel	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in response to applicant's communication filed September 11, 2006 in response to PTO office action mailed June 09, 2006. The applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to last office action, claims 1-3, 6-13 and 15 have been amended. No claims have been canceled. No claims have been added. As a result, claims 1-16 remain pending in this application.

Response to Arguments

3. Applicant argues that Shirotori applies enable signal to both ways and stops supplying signal to the data memories except to the one associated with the hit tag memory. The process of generating enable signal of Shirotori is dependent on the reference clocks (or access cycles) (fig. 3, col. 4, line 13 col. 5, line 7), this is similar to applicant's concept, "when the access cycle is slow enough to permit a single way to be clocked, and data is produced prior to the end of the access cycle, only one of the ways is (shown as way 0 in Fig. 2) clocked if a hit is determined" (see present application paragraph [0021]), Shiritori's teaching is similar to applicant's concept, "if the access controller 8 receives the hit information before the start signal, it supplies the enable signal only to the data memory 2 associated with the hit tag memory 1" and the further limitation of applying enable signal to both the memories is dependent on the access

cycle is not slow enough, the enable signal is applied to both the memories (col. 4, line 65 – col. 5, line 7), these statements clearly indicates that applying enable signal depends on access cycle.

4. Applicant's further arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. (US 6,356,990 B1) (Aoki herein after) and Shirotori et al. (5,920,888) (Shirotori herein after) and further in view of Santhanam et al. (US 2003/0149905 A1) (or Huang et al. "Customizing the Branch Predictor to Reduce Complexity and Energy Consumption" published by IEEE Computer Society, September-October, 2003)

As per claim 1, Aoki teaches a system for accessing a two-way associative cache having first and second ways (fig. 2), comprising:

an effective address register connected to simultaneously apply an address to each of said two-way associative cache (fig. 2, item 20, column 3, lines 5-14);

an output multiplexer for selecting data from one of first and second ways of said two way associative cache in response to a select signal identifying one of said ways of said associative cache (fig.2, item 25, column 3, lines 25-28); and

a byte select circuit configured to select an individual byte of the data selected by the output multiplexer in accordance with the byte data contained in the effective address register (column 3, lines 9-14).

Aoki fails to teach a clock circuit for selectively applying clock pulse in response to a mode access signal. Shirotori teaches a circuit for selectively applying start/enable signals to one or many ways of associative cache in response to a mode access signal [fig. 3, column 2, lines 8-16, col. 4, lines 13-8, taught as data memory allows reading data stored therein in response to enable signal and prohibits the same if the enable signal is stopped, further the operating mode (i.e. power efficiency or high speed access) is determined based on the operating frequencies (i.e. reference clocks), col. 4, lines 38-65, start signal is further used to enable the ways of the memory, fig. 3, the start signal is equivalent to mode select signal].

It would have been obvious to one having ordinary skill in the art at the time of the invention to utilize mode-switching circuit of Shirotori in the system of Aoki to automatically switch between high-speed access mode and power saving mode (Shirotori, column 1, lines 55-67).

wherein, in a power efficiency access mode, said select signal selects one of said first way and second way at an end of an access cycle [col. 4, line 65 – col. 5, line 7, Shirotori teaches, if the access controller receives hit information before the start

signal, it supplies the enable signal only to the data memory associated with the tag memory and hit data memory is read, this is similar to applicant's concept, "when the access cycle is slow enough to permit a single way to be clocked, and data is produced prior to the end of the access cycle, only one of the ways is (shown as way 0 in Fig. 2) clocked if a hit is determined" (see present application paragraph [0021])].

Shirotori teaches an enable signal but fails to teach applying selective clock signal. Santhanam teaches clock-gating circuit for selectively applying clocks to parts of digital circuits and applies clock signal to different cache banks (paragraphs [0006], [0007], [0055] and [0058]).

It would have been obvious to one having ordinary skill in the art at the time of the invention to selectively apply clock signal to enable cache banks (ways) as taught by Santhanam in the system of Aoki and Shirotori to reduce the power consumption (Santhanam, paragraph [0005], Huang also teaches selective application of clock gating to cache ways to reduce power consumption, see page 13, col. 1, paragraph 3).

As per claim 2, Aoki teaches a tag array connected to be addressed by said address circuit for storing first and second sets of tag signals corresponding to a corresponding set of data stored in said first and second ways (fig.2, item 22, column 2, lines 65-67, column 3, lines 1-4); and

first and second comparator connected to compare first and second output from said tag array with tag data derived from said address (fig. 2, item 24, column 3, lines 20-23),

thereby identifying one of said ways of said associative caches containing data to be read, said one comparator generating a select signal for said output multiplexer (fig.2, items sel_1 and sel_0, column 3, lines 25-28).

As per claim 3, Shirotori teaches control signal applies enable signal to both ways of said associative cache when the access time for reading said data from one of said sets is less than a predetermined amount (column 2, lines 54-57, column 6, lines 5-15) and Santhanam teaches clock signal to selectively enable cache ways (Santhanam, paragraphs [0055] and [0058]).

As per claim 4, Shirotori teaches access mode signal is generated from prediction logic, which predicts which of said first, and second ways of said two way associative cache contains said data (fig, 3, column 4, lines 40-67, column 5, lines 1-7).

As per claim 5, Shirotori teaches enable circuit receives data from said comparator identifying which of said ways of said associative cache is to be clocked (fig.3, column 5, lines 4-8) and Santhanam teaches clock gating circuit to selectively enable cache ways (Santhanam, paragraphs [0006], [0007], [0055] and [0058]).

As per claim 6, Shirotori teaches enable circuit receives an access mode signal, which indicates that both of said sets of associative cache are to be clocked simultaneously (fig.3, column 5, lines 1-4) and Santhanam teaches clock gating circuit to selectively enable cache ways (Santhanam, paragraphs [0006], [0007], [0055] and [0058]).

As per claim 7, Shirotori teaches access signal selected based upon a need to conserve power or to provide high-speed operation (column 2, lines 8-17).

Claims 8-11 are rejected under same rationales as applied to claims 1-7 above, as Aoki and Shirotori teaches a system for accessing a data cache (fig. 2 of Aoki and fig.3 of Shirotori) with tag memories, translation device, comparators and a multiplexer for selecting output data, a byte select circuit and a clock signal circuit as explained with respect claims 1-2 above. Shirotori teaches two access modes (claims 9-10) (column 2, lines 8-17) and access speed is one half of a maximum access speed (claim 11, column 2, lines 28-31, column 6, lines 20-37).

Claims 12-16 are rejected under same rationales and explanation provided for claims 1-11 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kaushikkumar Patel
Examiner
Art Unit 2188

kmp

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER

11/13/06